

WHAT IS CLAIMED IS:

1 1. A flip-flop comprising:

2 a mode configuration input for receiving a test enable signal for configuring the
3 flip-flop between a test mode of operation and a normal mode of operation;
4 at least one data input for receiving at least one data signal, said flip-flop being
5 capable of storing the at least one data signal when the flip-flop is in the normal mode
6 of operation;

7 a scan input for receiving a test data signal, said flip-flop being capable of storing
8 the test data signal when the flip-flop is in the test mode of operation;

9 a scan output; and

10 a circuit for enabling the scan output to output the logic value stored in the flip-
11 flop when the flip-flop is in the test mode of operation and for disabling the scan output
12 from outputting the logic value stored in the flip-flop when the flip-flop is in the normal
13 mode of operation.

1 2. The flip-flop of claim 1, further comprising at least one latch, said circuit
2 being coupled between the scan output and the at least one latch.

1 3. The flip-flop of claim 1, further comprising a data output for providing
2 the value stored in the flip-flop, said circuit being coupled between the data output and
3 the scan output.

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1 4. The flip-flop of claim 3, wherein the circuit comprises at least one pass
2 gate transistor coupled between the data output of the flip-flop and the scan output so
3 that the scan output selectively follows the data output of the flip-flop.

1 5. The flip-flop of claim 1, wherein the circuit drives said scan output to a
2 predetermined logic value when the flip-flop is in the normal mode of operation.

1 6. The flip-flop of claim 5, wherein the circuit comprises a pull down
2 transistor coupled to the scan output for selectively driving the scan output to a low logic
3 value.

1 7. The flip-flop of claim 5, wherein the circuit comprises a pull up transistor
2 coupled to the scan output for selectively driving the scan output to a high logic value.

1 8. The flip-flop of claim 1, wherein the flip-flop is a D-flip-flop.

1 9. The flip-flop of claim 1, further comprising a data output for outputting
2 the logic value stored in the flip-flop, wherein the circuit comprises a logic gate having
3 a first input coupled to a data output of the flip-flop and an output coupled to the scan
4 output for generating an output logic value.

1 10. The flip-flop of claim 9, wherein a second input of the logic gate is
2 coupled to the mode configuration input.

1 11. An integrated circuit configured to operate in a normal mode of operation
2 and a test mode of operation, said integrated circuit comprising:

3 a plurality of registers selectively connected together to form at least one serial
4 shift register when the integrated circuit is configured in the test mode of operation, each
5 of the registers including at least one flip-flop, said at least one flip-flop within each of
6 the registers including at least a test enable input, a scan input, a data input, a scan
7 output and a data output;

8 a combinational logic circuit for receiving as input the data output of the at least
9 one flip-flop within a first of the registers and for generating a signal coupled to the data
10 input of the at least one flip-flop within a second of the registers;

11 wherein the at least one flip-flop in each of the registers is enabled for storing the
12 signal appearing on the scan input of the at least one flip-flop and disabled from storing
13 the signal appearing on the data input of the at least one flip-flop when the integrated
14 circuit is in the test mode of operation, disabled from storing the signal appearing on the
15 scan input of the at least one flip-flop and enabled for storing the signal appearing on the
16 data input of the at least one flip-flop when the integrated circuit is in the normal mode
17 of operation, and enabled to output a logic value stored by the at least one flip-flop on
18 the scan output of the at least one flip-flop when in the test mode of operation and
19 disabled from outputting on the scan output the logic value stored by the at least one
20 flip-flop when in the normal mode of operation.

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1 12. The integrated circuit of claim 11, wherein said at least one flip-flop of
2 each register comprises at least one pass gate transistor coupled between the data output
3 and the scan output of the flip-flop for selectively providing, by the scan output, the logic
4 value stored by the flip-flop.

1 13. The integrated circuit of claim 11, wherein the scan output of the at least
2 one flip-flop of each register is driven to a predetermined logic value when in the normal
3 mode of operation.

1 14. The integrated circuit of claim 13, wherein the at least one flip-flop of
2 each register comprises a transistor coupled to the scan output for driving the scan
3 output to the predetermined logic value.

1 15. The integrated circuit of claim 11, wherein the at least one flip-flop of
2 each register comprises a logic gate having a first input coupled to a data output of the
3 flip-flop, a second input of the logic gate coupled to the test enable input and an output
4 coupled to the scan output.

1 16. A method for testing an integrated circuit having a plurality of registers
2 therein, each one of the registers including at least one register bit having a scan output,
3 said method comprising the steps of:

4 configuring the registers to form at least one serial shift register using the scan
5 output of each register bit;

6 shifting a test pattern into the at least one serial shift register;

7 configuring the registers in a normal mode of operation, including disabling the
8 scan output of at least some register bits so that for each of the at least some register
9 bits, the scan output thereof is disabled from providing a value indicative of a value
10 maintained by the register bit; and

11 applying at least one clock cycle to the registers.

1 17. The method of claim 16, wherein the step of configuring the registers in
2 a normal mode of operation comprises the step of driving the scan output of at least
3 some of the register bits to a predetermined logic value.

1 18. The method of claim 16, further comprising repeating the steps of
2 configuring the registers to form at least one serial shift register chain, shifting,
3 configuring the registers in a normal mode of operation, and applying the at least one
4 clock cycle for different test patterns a number of times.

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1 19. The method of claim 18, further comprising, following the step of
2 repeating, the step of:

3 configuring the registers in a normal mode of operation, including disabling the
4 scan output of the at least some register bits and driving the scan output to the
5 predetermined logic value.

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1 20. A method for operating a flip-flop having serial scan capabilities including
2 a scan output, said method comprising the steps of:

3 receiving a mode configuration signal for configuring the flip-flop between a test
4 mode of operation and a normal mode of operation; and

5 selectively disabling the scan output from providing the logic value stored by the
6 flip-flop based upon the value of the mode configuration signal received.

1 21. The method of claim 20, further comprising:

2 selectively driving the scan output to a predetermined logic value based upon the
3 value of the mode configuration signal received.

1 22. The method of claim 21, wherein the step of driving comprises driving
2 the scan output to a low logic value.

1 23. The method of claim 21, wherein the step of driving comprises driving
2 the scan output to a high logic value.

1 24. The flip-flop of claim 20, wherein the logic value stored in the flip-flop
2 corresponds to an output of the flip-flop.

1 25. The flip-flop of claim 20, wherein the step of selectively disabling is
2 performed when said mode configuration signal configures the flip-flop in the normal
3 mode of operation.